What is Claimed Is:

1. A method in a Fast Fourier Transform (FFT) circuit having at least a Radix-4 butterfly element, the method including:

storing first and second equal portions of a prescribed number of data values in first and second memory portions, respectively, according to a prescribed mapping that ensures the first and second memory portions are accessed for each in-place computation operation;

executing a prescribed number of FFT stages each having a prescribed number of the in-place computation operations relative to the prescribed number of data values, wherein the executing step includes performing each in-place computation operation by:

(1) concurrently accessing an equal number of stored data values from the first memory portion and the second memory portion; and

(2) supplying the accessed data values to the at least Radix-4 butterfly element for calculation of respective calculation results.

2. The method of claim 1, wherein the step of performing each in-place computation includes storing the calculation results in the first memory portion and the second memory portions at memory locations having stored the respective accessed data values.

3. The method of claim 2, wherein the first and second memory portions each are dual-port memory devices, the executing step including accessing the stored data values for a subsequent one of the in-place computation operations concurrently during the storing of the calculation results for said each in-place computation operation.

4. The method of claim 3, wherein the executing step includes performing the in-place computation operations for a first of the FFT stages in a prescribed order based on an input sequence of one of the in-place operations for a second of the FFT stages.

5. The method of claim 4, wherein the executing step further includes initiating the one in-place operation for the second of the FFT stages after having completed the prescribed order of the in-place computation operations relative to the input sequence.

6. The receiver of claim 2, wherein the concurrently accessing step includes accessing, for each clock cycle, a corresponding stored data value from a read port of the first memory portion

and a corresponding stored data value from a read port of the second memory portion, the storing step including writing, during said each clock cycle, a corresponding calculation result via a write port of the first memory portion and a corresponding calculation result via a write port of the second memory portion.

7. A Fast Fourier Transform (FFT) circuit comprising:

at least a Radix-4 butterfly element configured for generating calculation results in response to receipt of accessed data values;

first and second memory portions configured for storing first and second equal portions of a prescribed number of data values for in-place computation operations; and

a memory controller configured for storing the first and second equal portions of the prescribed number of data values in the first and second memory portions, respectively, according to a prescribed mapping that ensures the first and second memory portions are accessed for each in-place computation operation, the memory controller configured for executing a prescribed number of FFT stages, each having a prescribed number of the in-place computation operations relative to the prescribed number of data values, based on:

(1) concurrently accessing an equal number of stored data values from the first memory portion and the second memory portion; and

(2) supplying the accessed data values to the at least Radix-4 butterfly element for calculation of the respective calculation results.

8. The FFT circuit of claim 7, wherein the memory controller is configured for storing the calculation results for each in-place computation operation in the first memory portion and the second memory portions at memory locations having stored the respective accessed data values.

9. The FFT circuit claim 8, wherein the first and second memory portions each are dual-port memory devices, the memory controller configured for accessing the stored data values for a subsequent one of the in-place computation operations concurrently during the storing of the calculation results for said each in-place computation operation.

10. The FFT circuit of claim 9, wherein the memory controller configured for causing executing of the in-place computation operations for a first of the FFT stages in a prescribed order based on an input sequence of one of the in-place operations for a second of the FFT stages.

11. The FFT circuit of claim 10, wherein the memory controller is configured for initiating the one in-place operation for the second of the FFT stages after having completed the prescribed order of the in-place computation operations relative to the input sequence.

12. The FFT circuit of claim 8, wherein the memory controller is configured for accessing, for each clock cycle, a corresponding stored data value from a read port of the first memory portion and a corresponding stored data value from a read port of the second memory portion, the memory controller configured for writing, during each clock cycle following generation of calculation results by the at least Radix-4 butterfly, a corresponding calculation result via a write port of the first memory portion and a corresponding calculation result via a write port of the second memory portion.